CHT-7474 DATASHEET

Revision: 03.7
15-Feb-21
(Last Modified Date)

High-Temperature, Dual D-Flip-Flop

General Description

The CHT-7474 is a dual positive-edge-triggered D type Flip-flop. Data on the D input is transferred to the output on a rising edge of the clock impulse.
Rn and Sn are asynchronous reset and set. On a low state, they operate on the outputs regardless of the other inputs.

This circuit is designed assuring latchup-free operation for all supply and temperature conditions.

The CHT-7474 can operate with supply voltages from 3.3 to 5V (±10%).

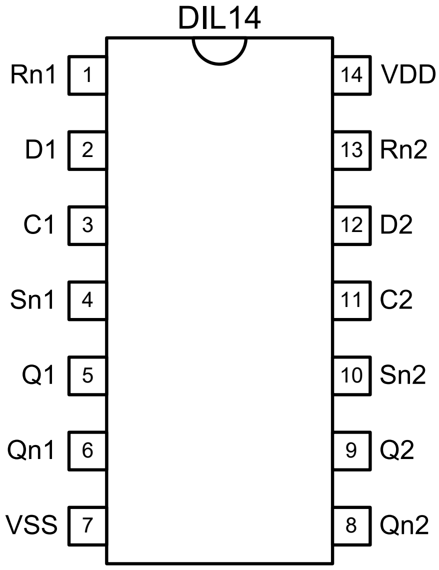
Features

- Qualified from -55 to +225°C (Tj)
- 3.3 to 5V (±10%) supply voltages
- Latchup-free at any supply and temperature condition
- Validated at 225°C for 30000 hours (CDIL14) and 20000 hours (CSOIC16) (and still on-going)
- Available in DIL14and CSOIC16 hermetic standard package

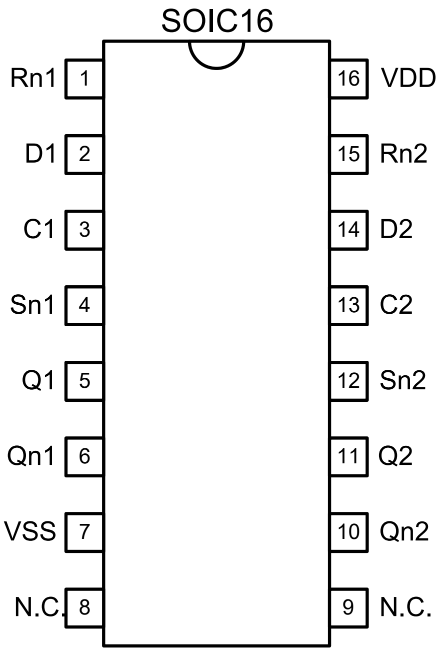
Applications

- Well logging,
- Automotive, Aeronautics & Aerospace
- Harsh Environments

Package and Pin Configuration



Pin	Symbol	Description
1	**RN1**	Reset of D-flip-flop 1
2	**D1**	Input of D-flip-flop 1
3	**C1**	Clock pulse of D-flip-flop 1
4	**SN1**	Set of D-flip-flop 1
5	**Q1**	Output of D-flip-flop 1
6	**QN1**	Inverted output of D-flip-flop 1
7	**GND**	Circuit core ground terminal.
8	**QN2**	Inverted output of D-flip-flop 2
9	**Q2**	Output of D-flip-flop 2
10	**SN2**	Set of D-flip-flop 2
11	**C2**	Clock pulse of D-flip-flop 2
12	**D2**	Input of D-flip-flop 2
13	**RN2**	Reset of D-flip-flop 2
14	**VDD**	Circuit core power supply terminal.



Pin	Symbol	Description
1	**RN1**	Reset of D-flip-flop 1
2	**D1**	Input of D-flip-flop 1
3	**C1**	Clock pulse of D-flip-flop 1
4	**SN1**	Set of D-flip-flop 1
5	**Q1**	Output of D-flip-flop 1
6	**QN1**	Inverted output of D-flip-flop 1
7	**VSS**	Circuit core ground terminal.
8	**NC**	Not connected
9	**NC**	Not connected
10	**QN2**	Inverted output of D-flip-flop 2
11	**Q2**	Output of D-flip-flop 2
12	**SN2**	Set of D-flip-flop 2
13	**C2**	Clock pulse of D-flip-flop 2
14	**D2**	Input of D-flip-flop 2
15	**RN2**	Reset of D-flip-flop 2
16	**VDD**	Circuit core power supply terminal.

Function Table

INPUT				OUTPUT	
Sn	**Rn**	**C**	**D**	**Q**	**Qn**
L	**H**	**X**	**X**	**H**	**L**
H	**L**	**X**	**X**	**L**	**H**
L	**L**	**X**	**X**	**L**	**X**[1]
Sn	**Rn**	**C**	**D**	**Q(n+1)**	**Qn(n+1)**
H	**H**	↑	**L**	**L**	**H**
H	**H**	↑	**H**	**H**	**L**

[1] Having Sn=Rn=LOW at the same time should be avoided. The only known output is Q.

Logical Diagram

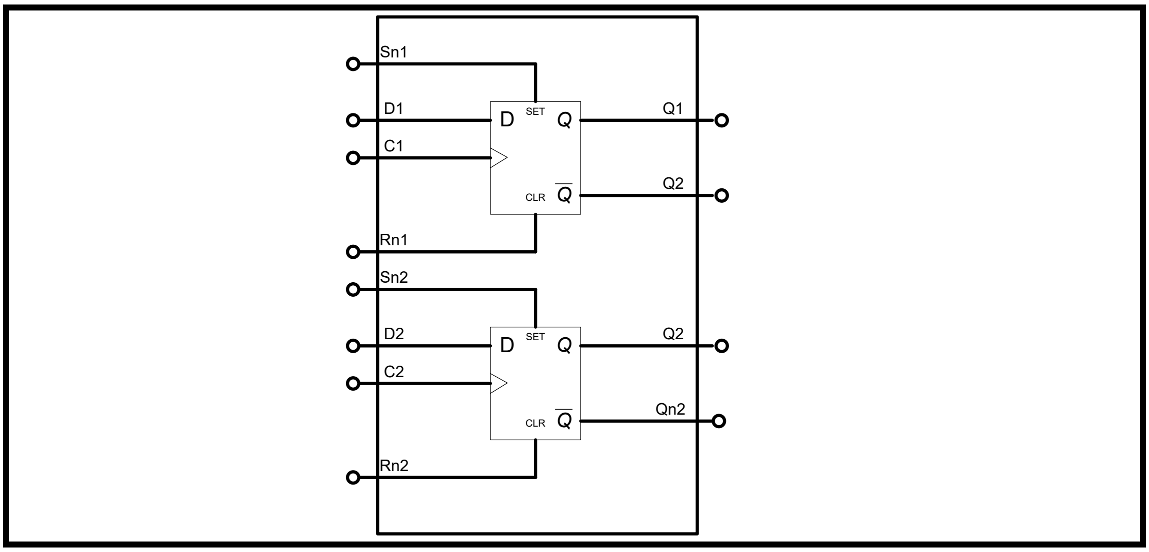


Figure 1. CHT-7474: simplified logical diagram.

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND -0.5 to 6.0V
Voltage on any Pin to GND -0.5 to V_{DD}+0.5V

ESD Rating (expected)
Human Body Model 1kV

Operating Conditions

Supply Voltage V_{DD} to GND 3.3V to 5V (±10%)
Junction temperature -55°C to +225°C

DC Electrical Characteristics

Unless otherwise stated: VDD=5V, T_j=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage **V_{DD}**		2.97		5.5V	V
Quiescent current **I_{DD}**	V_{DD} = 3.3V, T_j=-55°C			20	nA
	V_{DD} = 5V, T_j=-55°C			20	
	V_{DD} = 3.3V, T_j=225°C			**<u>2650</u>**	
	V_{DD} = 5V, T_j=225°C			**<u>3030</u>**	
Minimum HIGH level output voltage **V_{OH}**	V_{DD} = 3.3V, I_{OH}<4mA (source)	**<u>2.7</u>**	3.04		V
	V_{DD} = 5V, I_{OH}<4mA (source)	**<u>4.6</u>**	4.82		
Maximum LOW level output voltage **V_{OL}**	V_{DD} = 3.3V, I_{OL}<4mA (sink)		0.28	**<u>0.5</u>**	V
	V_{DD} = 5V, I_{OL}<4mA (sink)		0.20	**<u>0.4</u>**	
Minimum HIGH level input voltage **V_{IH}**	V_{DD} = 3.3V	**<u>2.4</u>**	2.10		V
	V_{DD} = 5V	**<u>3.7</u>**	3.49		
Maximum LOW level input voltage **V_{IL}**	V_{DD} = 3.3V		1.72	**<u>1.5</u>**	V
	V_{DD} = 5V		2.16	**<u>2.0</u>**	
Input leakage current (source / sink) **± I_I**	VI=VCC or GND, V_{DD} = 3.3V		±1	**<u>±35</u>**	nA
	VI=VCC or GND, V_{DD} = 5V		±2	**<u>±37</u>**	

AC Electrical Characteristics

Unless otherwise stated: VDD=5V, T_j=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay from C to Q, Qn **t_{PHL}**	C_L=50pF	T_j=-55°C		12	21	ns
		T_j=25°C		14	25	
		T_j=225°C		19	33	
Propagation delay from Rn to Q, Qn **t_{PHL}**	C_L=50pF	T_j=-55°C		11	20	ns
		T_j=25°C		12	21	
		T_j=225°C		17	30	
Propagation delay from C to Q, Qn **t_{PLH}**	C_L=50pF	T_j=-55°C		9	16	ns
		T_j=25°C		10	18	
		T_j=225°C		15	27	
Propagation delay from Sn to Q, Qn **t_{PLH}**	C_L=50pF	T_j=-55°C		11	20	ns
		T_j=25°C		12	21	
		T_j=225°C		18	32	
Output transition time High to Low **t_{THL}**	C_L=50pF	T_j=-55°C		13	17	ns
		T_j=25°C		14	18	
		T_j=225°C		17	**<u>22</u>**	
Output transition time High to Low **t_{TLH}**	C_L=50pF	T_j=-55°C		19	25	ns
		T_j=25°C		20	26	
		T_j=225°C		23	**<u>30</u>**	
Clock pulse width **t_w**	C_L=50pF	T_j=-55°C	4	2		ns
		T_j=25°C	4	2		
		T_j=225°C	**<u>6</u>**	3		
Set or reset pulse width **t_w**	C_L=50pF	T_j=-55°C	4	2		ns
		T_j=25°C	4	2		
		T_j=225°C	**<u>6</u>**	3		
Removal time set or reset **t_{rem}**	C_L=50pF	T_j=-55°C	4	2		ns
		T_j=25°C	4	2		
		T_j=225°C	**<u>6</u>**	3		
Set-up time D to C **t_{su}**	C_L=50pF	T_j=-55°C	2	1		ns
		T_j=25°C	2	1		
		T_j=225°C	**<u>2</u>**	1		
Hold time C to D t_h	C_L=50pF	T_j=-55°C	**<u>2</u>**	1		ns
		T_j=25°C	2	1		
		T_j=225°C	2	1		
Maximum clock pulse frequency f_{max}	C_L=50pF	T_j=-55°C	31	63		MHz
		T_j=25°C	27	55		
		T_j=225°C	21	40		

AC Electrical Characteristics (cntd)

Unless otherwise stated: VDD=3.3V, T_j=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay from C to Q, Qn t_{PHL}	C_L=50pF	T_j=-55°C		23	40	ns
		T_j=25°C		26	45	
		T_j=225°C		35	61	
Propagation delay from Rn to Q, Qn t_{PHL}	C_L=50pF	T_j=-55°C		21	37	ns
		T_j=25°C		23	40	
		T_j=225°C		31	54	
Propagation delay from C to Q, Qn t_{PLH}	C_L=50pF	T_j=-55°C		17	30	ns
		T_j=25°C		20	35	
		T_j=225°C		26	45	
Propagation delay from Sn to Q, Qn t_{PLH}	C_L=50pF	T_j=-55°C		21	37	ns
		T_j=25°C		24	42	
		T_j=225°C		32	55	
Output transition time High to Low t_{THL}	C_L=50pF	T_j=-55°C		20	26	ns
		T_j=25°C		21	28	
		T_j=225°C		27	**<u>36</u>**	
Output transition time Low to High t_{TLH}	C_L=50pF	T_j=-55°C		23	30	ns
		T_j=25°C		24	32	
		T_j=225°C		26	**<u>34</u>**	
Clock pulse width t_w	C_L=50pF	T_j=-55°C	6	3		ns
		T_j=25°C	8	4		
		T_j=225°C	**<u>10</u>**	5		
Set or reset pulse width t_w	C_L=50pF	T_j=-55°C	6	3		ns
		T_j=25°C	8	4		
		T_j=225°C	**<u>10</u>**	5		
Removal time set or reset t_{rem}	C_L=50pF	T_j=-55°C	6	3		ns
		T_j=25°C	6	3		
		T_j=225°C	**<u>8</u>**	4		
Set-up time D to C t_{su}	C_L=50pF	T_j=-55°C	4	2		ns
		T_j=25°C	4	2		
		T_j=225°C	**<u>4</u>**	2		
Hold time C to D t_h	C_L=50pF	T_j=-55°C	**<u>2</u>**	-1		ns
		T_j=25°C	2	-1		
		T_j=225°C	2	-2		
Maximum clock pulse frequency f_{max}	C_L=50pF	T_j=-55°C	18	35		MHz
		T_j=25°C	16	31		
		T_j=225°C	**<u>12</u>**	24		

AC Waveforms

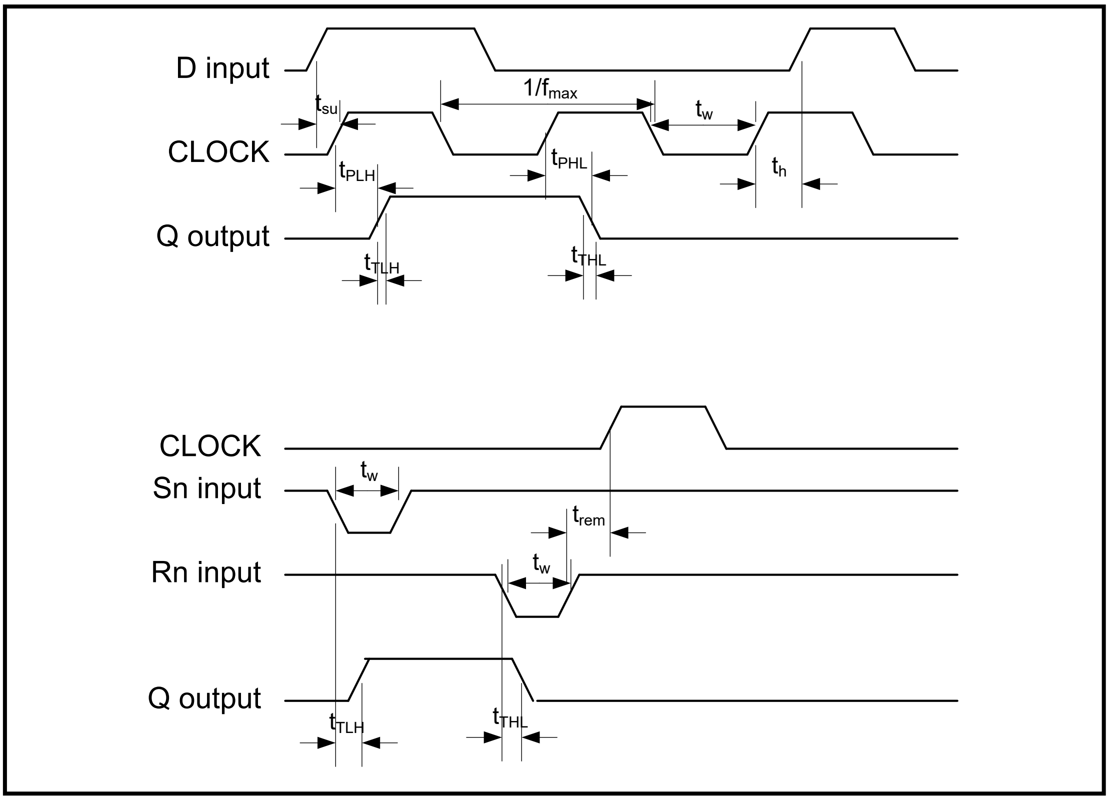
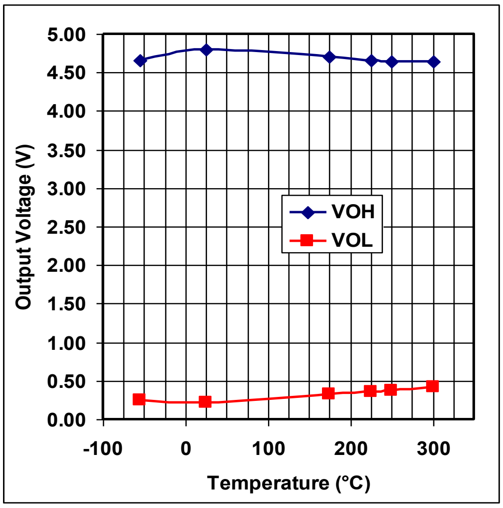
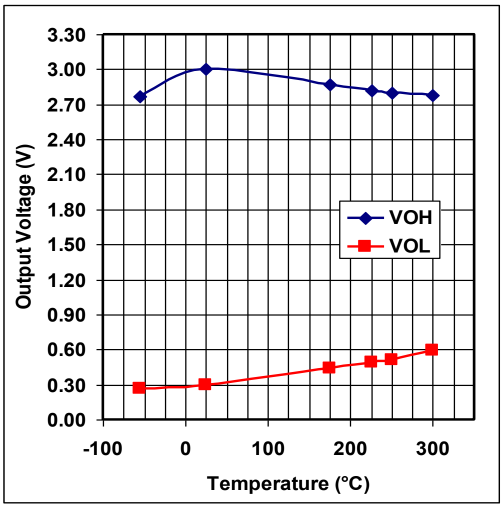


Figure 2. AC Waveforms

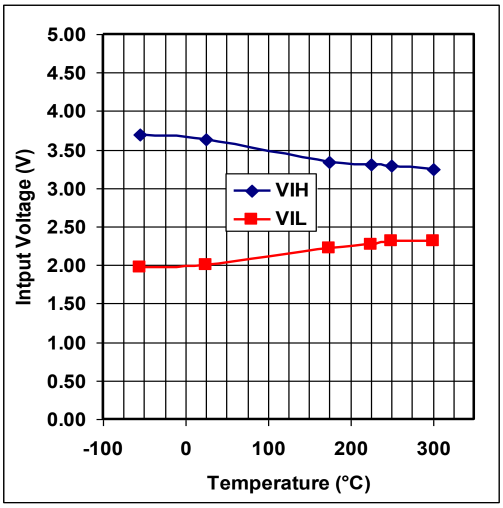
Typical Performance Characteristics



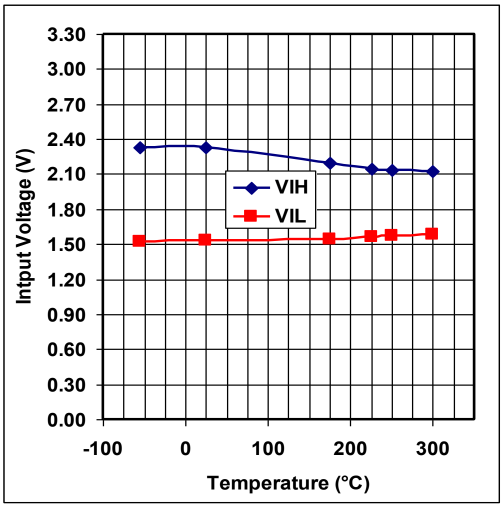
Output voltage levels versus temperature, V_{DD} = 5V



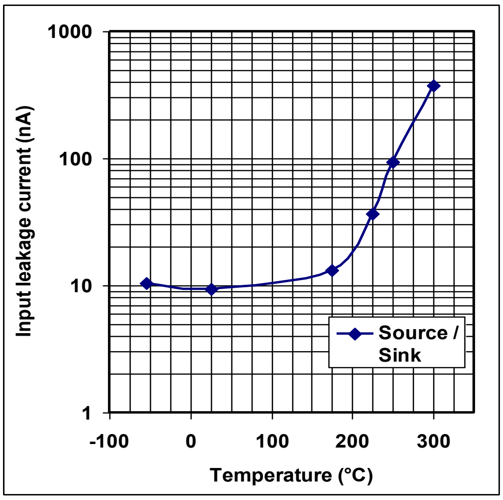
Output voltage levels versus temperature, V_{DD} = 3.3V



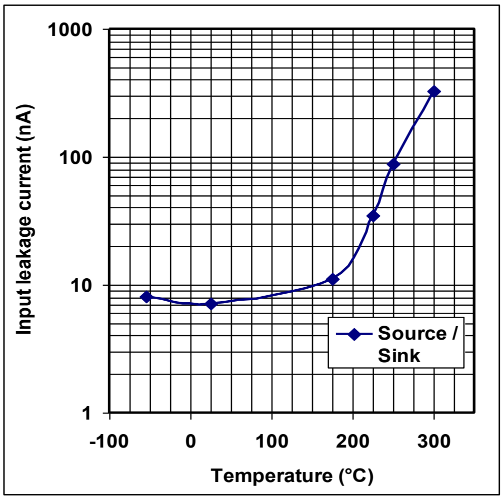
Input voltage levels versus temperature, V_{DD} = 5V



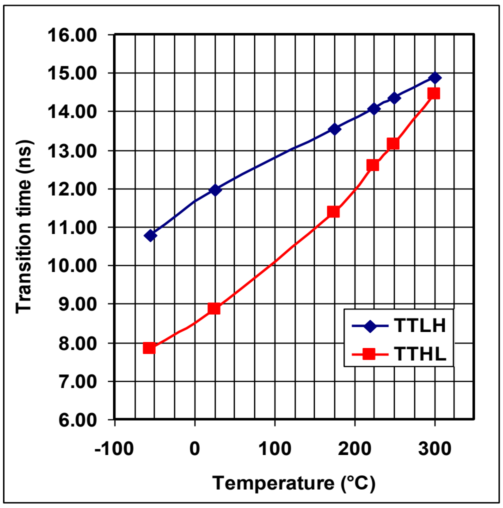
Input voltage levels versus temperature, V_{DD} = 3.3V



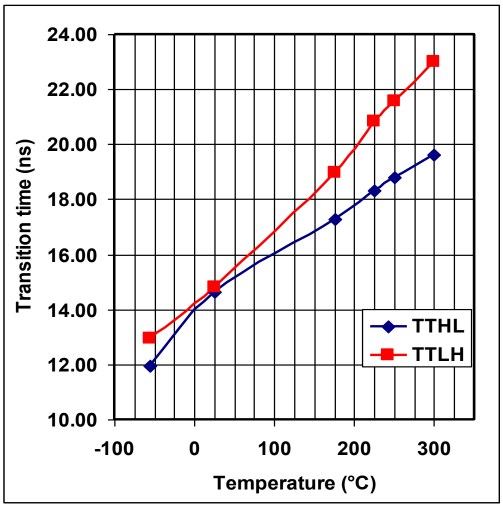
Input leakage current versus temperature, V_{DD} = 5V



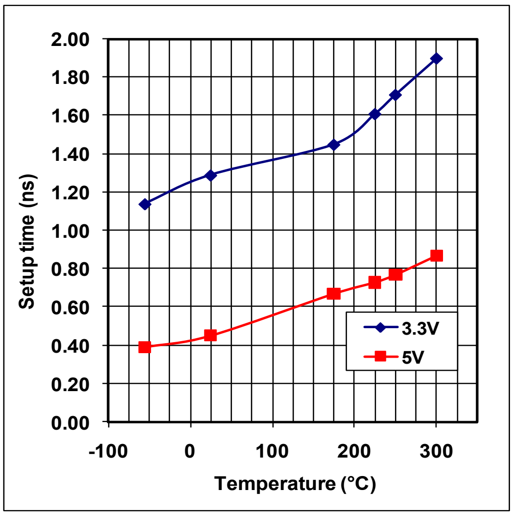
Input leakage current versus temperature, V_{DD} = 3.3V



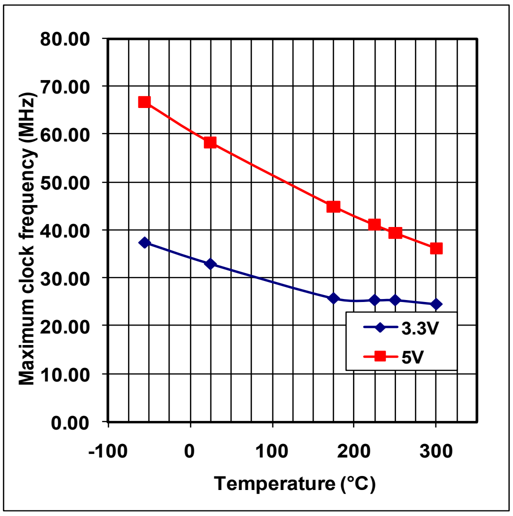
Transition times versus temperature, V_{DD} = 5V



Transition times versus temperature, V_{DD} = 3.3V



Setup time versus temperature, V_{DD} = 3.3V / 5V

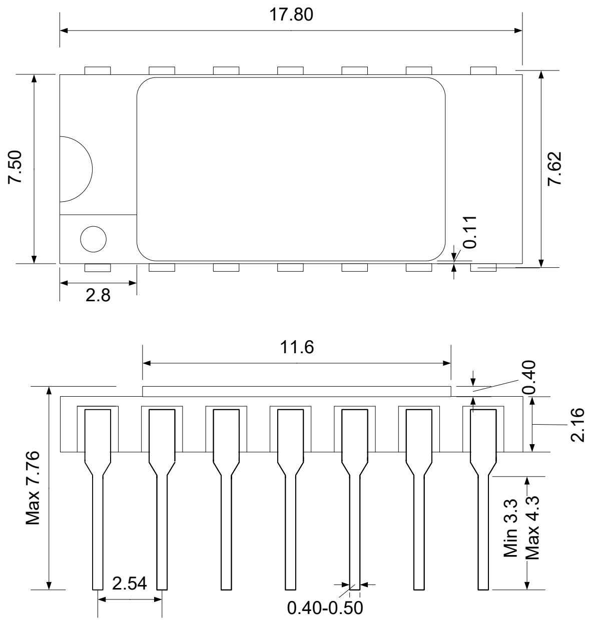


Maximum clock frequency versus temperature, V_{DD} = 3.3V / 5V

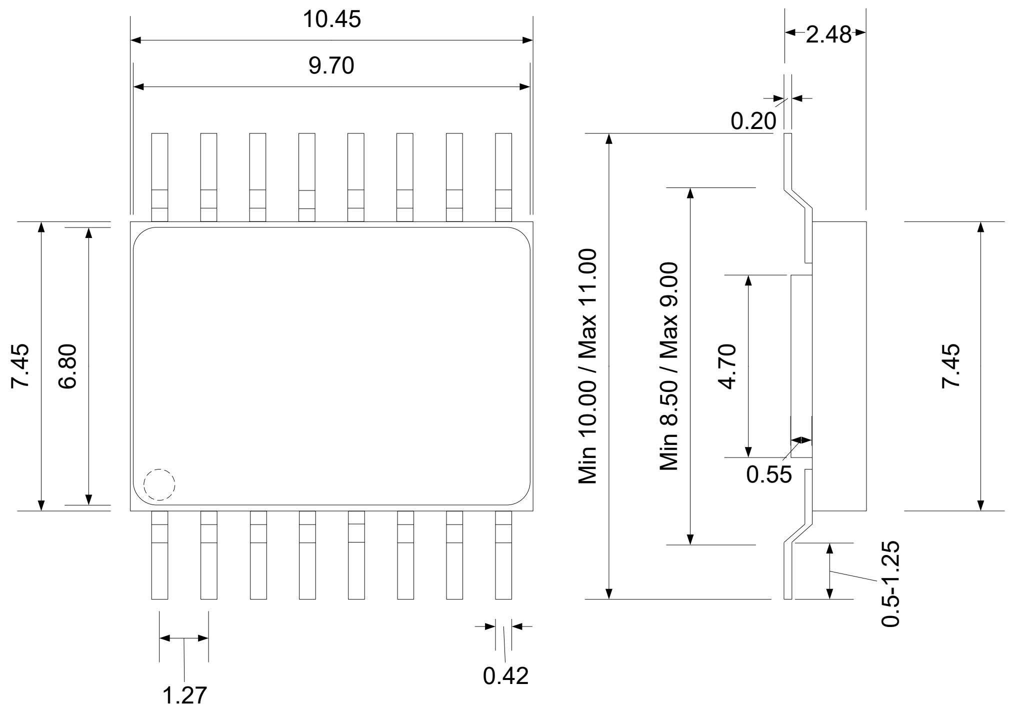
Ordering Information

Ordering Reference	Package	Temperature Range	Marking	Status
CHT-7474-CDIL14-T	Ceramic DIL14	-55°C to +225°C	CHT-7474	Not for new design
CHT-7474-CSOIC16-T	Ceramic SOIC16	-55°C to +225°C	CHT-7474	Active

Package Dimensions



Drawing CDIL14 (mm +/- 10%)



Drawing CSOIC16 (mm +/- 10%)