ISOCOM LIMITED

PART NUMBER

COMPONENT SPECIFICATION

CSMRLVGXXP1

ISSUE 2

Component Specification
For Hermetically Sealed, Radiation-Hard
Latching Solid State Relay

Features	Applications
▪ Low on-state resistance	▪ Designed for 10 to 50V$_{DC}$ Bus Application
▪ Selection of Operating Current and Voltage	▪ Space Systems/Satellites
▪ SPST, SPDT, DPST, DPDT	▪ Space Battery Management Systems
▪ Full Military temperature range -55°C - +125°C	▪ Bus Control
▪ Military and Space Screening	▪ Aerospace Power Distribution
▪ Compatible with µC Drive	▪ Power Isolation and Control
▪ Internally Isolated	
▪ Output Currents up to 20A	

DESCRIPTION

ISOCOM Latching Solid State Relays are designed to replace existing electro-mechanical relays (EMR). The CSMRLVGXXP1 is available in either the single pole single throw (SPST) or single pole double throw (SPDT) configuration. They are resilient to damage from shock and immune to contact-related problems (arcing, contamination) that are associated with mechanical equivalents. They are also lightweight in comparison to the EMR. Coupling between the input, output and power bus stages offers an effective isolation up to 500V. The latch and reset input stages are designed to directly interface with standard microcontrollers (µC), requiring low current (< 10mA) 3.3V or 5V logic. This device offers various operating voltage ranges from 10 to 50V with current capabilities up to 20A. Furthermore, it is featured in an 8-Lead Surface Mount package where each pin is isolated with a glass seal. This hermetic ceramic package comes with a gold plate finish and solder dip options available.

ISOCOM Limited is AS9100 certified for the design and manufacture of electronic and optoelectronic components.

STANDARDS

The following specifications have been complied with in the manufacturing of this product –

Aerospace Compliance Standards

AS9100D & ISO 9001:2015 – Design & Manufacture of Electronic and Optoelectronic Components *(Ref GB15/92780)*

Military Compliance Specifications

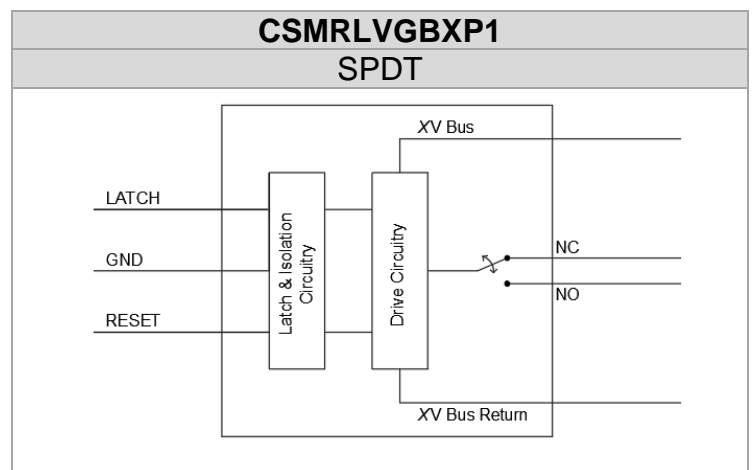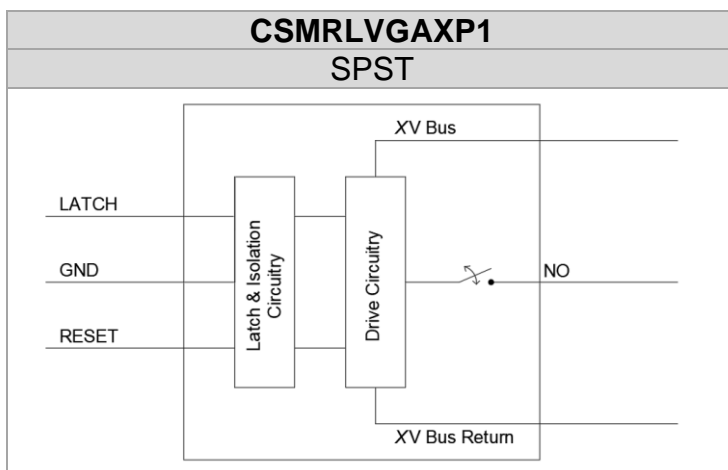MIL-PRF-28750 – General Specification for Solid State Relay

Military Compliance Standards

MIL-STD-883 – Test Method Standard Microcircuits

SCREENING INFORMATION

Our LSSR range can be screened to MIL-PRF-28750, applying test methods from MIL-STD-883. Please contact us for more information relating to the applicable screening processes.

FUNCTIONAL DIAGRAMS

CSMRLVGAXP1
SPST

CSMRLVGBXP1
SPDT

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C U.O.S

Storage Temperature	-65° to +150°C
Operating Temperature	-55° to +125°C
Soldering Temperature	260°C
Continuous Output Current per relay – I_O	See Selection Guide *
Output Voltage- V_O	See Selection Guide +10%
V_{LATCH}	7V
V_{RESET}	7V
I_{LATCH}	15mA
I_{RESET}	15mA
Input-to-Output Isolation Voltage	⇑500 V_{DC}
XVBus	50V

*Current Limited by Package

ELECTRICAL CHARACTERISTICS

T_A= -55°C to +125°C U.O.S

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
Latch voltage	V_{Latch}	I_{Latch} = 10mA	3	5	-	V
Reset voltage	V_{Rst}	I_{Rst} = 10mA				
Latch Current	I_{Latch}	V_{Latch} = 5V	7	10	-	mA
Reset Current	I_{Rst}	V_{Rst} = 5V				
Latch/Reset reverse breakdown voltage	$B_{VR(Latch)}$ $B_{VR(Rst)}$	I_R = 10 μA	5	-	-	V
Latch pulse duration	PW_{Latch}	V_{Latch} = 5V	40	-	-	μs
Reset pulse duration	PW_{Rst}	V_{Rst} = 5V	40	-	-	μs
Output						
XVBus current	$I_{Bus\,(Latched)}$	X = 10V to 50V, mode = Latch	-	8	-	mA
	$I_{Bus(Unlatched)}$	X = 10V to 50V, mode = Reset	-	1.5	-	mA
Output current	I_O		See selection guide (Page 7)			A
Output on state resistance (per output)	$R_{(On)}$	X = 10V to 50V				mΩ
Output leakage Current	I_{OL}		-	10	100	μA
Coupled						
Input-to-output isolation breakdown voltage [1]	V_{I-O}	I_{I-O} in to out = 1μA, T_A = 25°C	-	-	500	V
Latch time (NO Latch) [2]	$T_{PL(NO)}$		-	950	-	μs
Latch time (NC Latch) [2]	$T_{PL(NC)}$	X = 10V TO 50V, I_{OX} = See selection guide	-	150	-	
Reset latch delay (NO to reset) [2]	$T_{PR(NO)}$		-	250	-	
Reset latch delay (NC to reset) [2]	$T_{PR(NC)}$		-	150	-	

Notes:
(1) Inputs shorted together; outputs shorted together
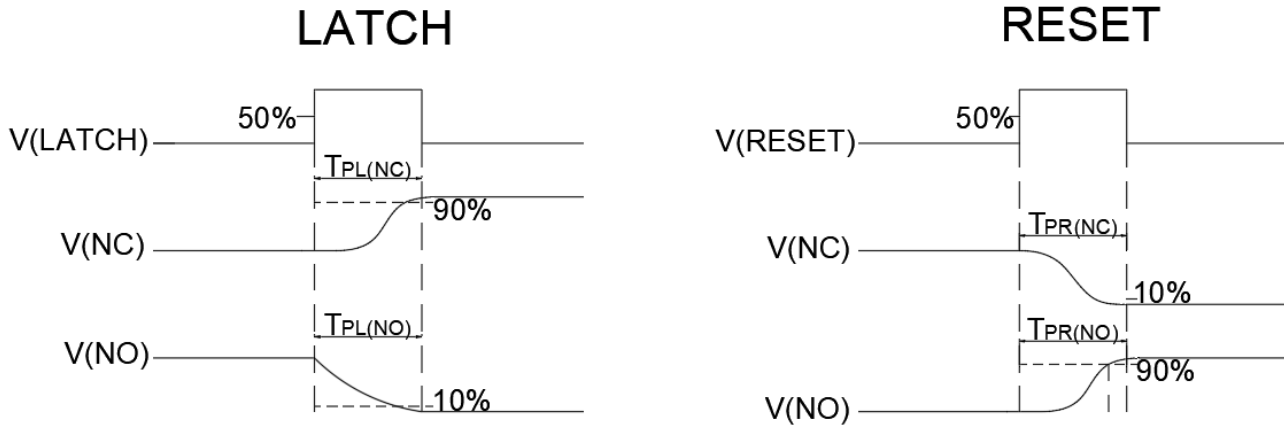(2) See propagation timing delay measurements

For sales enquiries, or further information, please contact our sales office at –

ISOCOM Limited • 2 Fern Court • Bracken Hill Business Park • Peterlee • County Durham • SR8 2RR• United Kingdom

Email: sales@isocom.uk.com • Tel: +44 (0)191 416 6546

PROPAGATION TIMING DELAY MEASUREMENTS

Switching Characteristics (Note: All Signals Measured with Respect to XV Bus Return)

TRUTH TABLE

Bus Voltage	on	on	on	on	on	on	off	on
Latch	0	1	0	0	0	1	X	0
Reset	0	0	0	1	0	0	X	0
NO status	Open	Closed	Closed	Open	Open	Closed	Open	Open
NC status	Closed	Open	Open	Closed	Closed	Open	Open	Closed

On initial powerup the LSSR is in its default condition. The normally open (NO) and normally closed (NC) outputs are open and closed respectively. Upon receiving a short input pulse to the LATCH input, the NO and NC terminals become closed and open circuit respectively. The device will then remain in the latched condition indefinitely or until a short input pulse to the RESET returns the outputs to their default conditions. Additionally, if the XV bus line is off while the LSSR is in the LATCH state, the device outputs automatically return to their default conditions upon the power reinstatement.
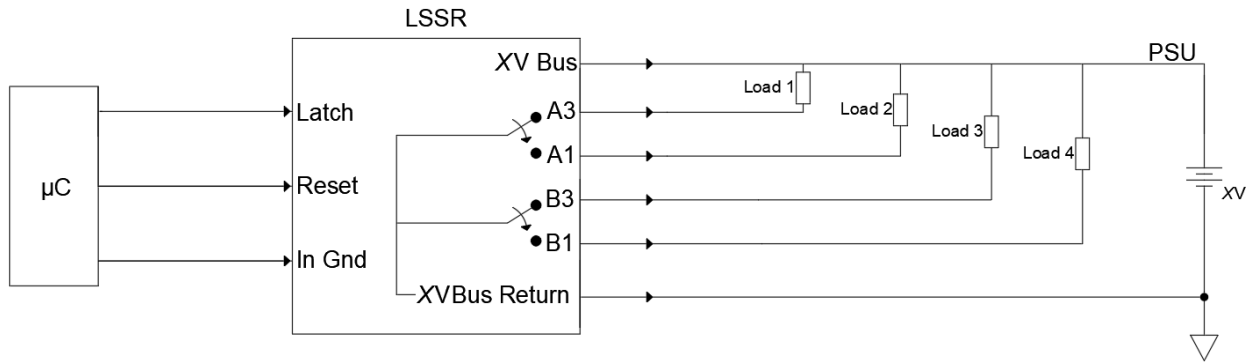
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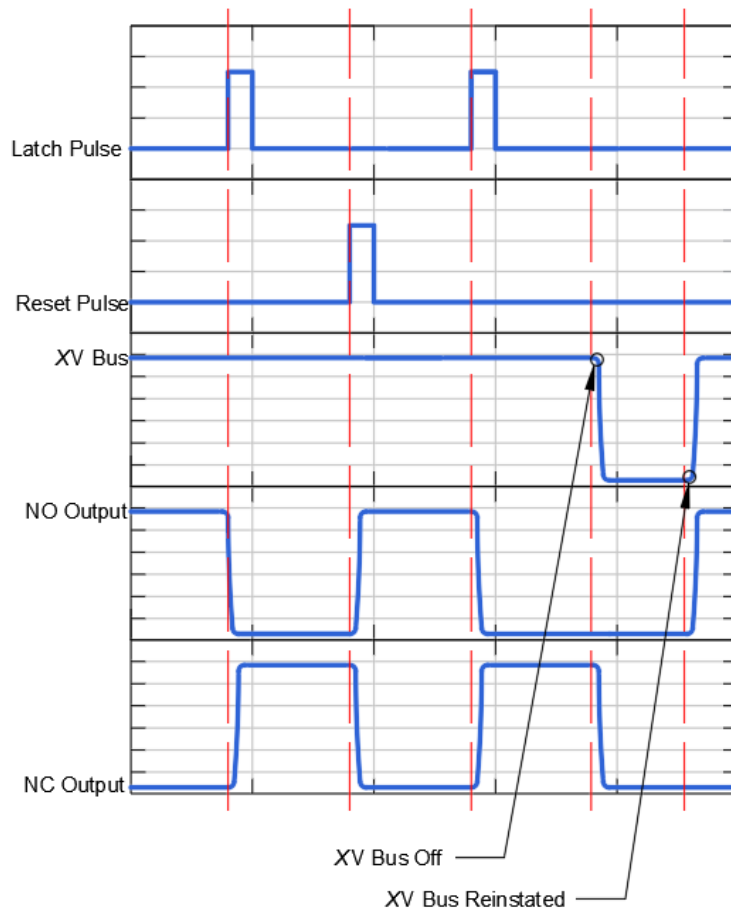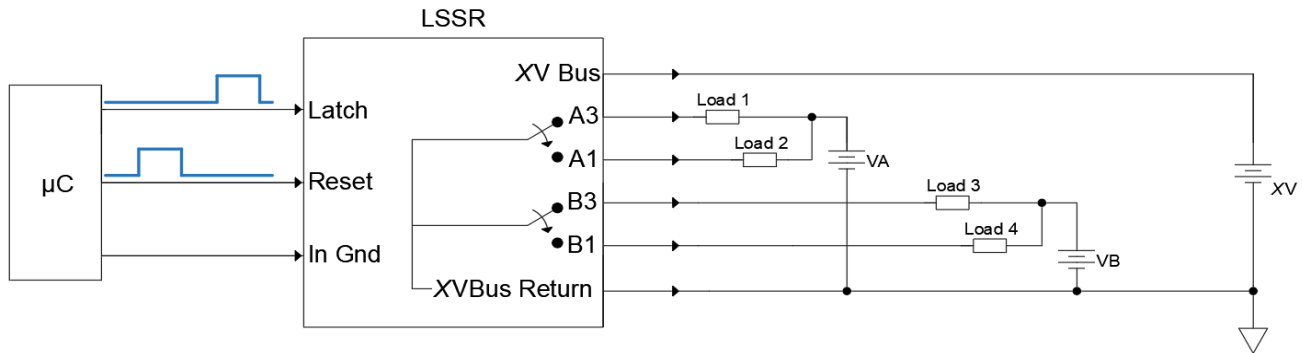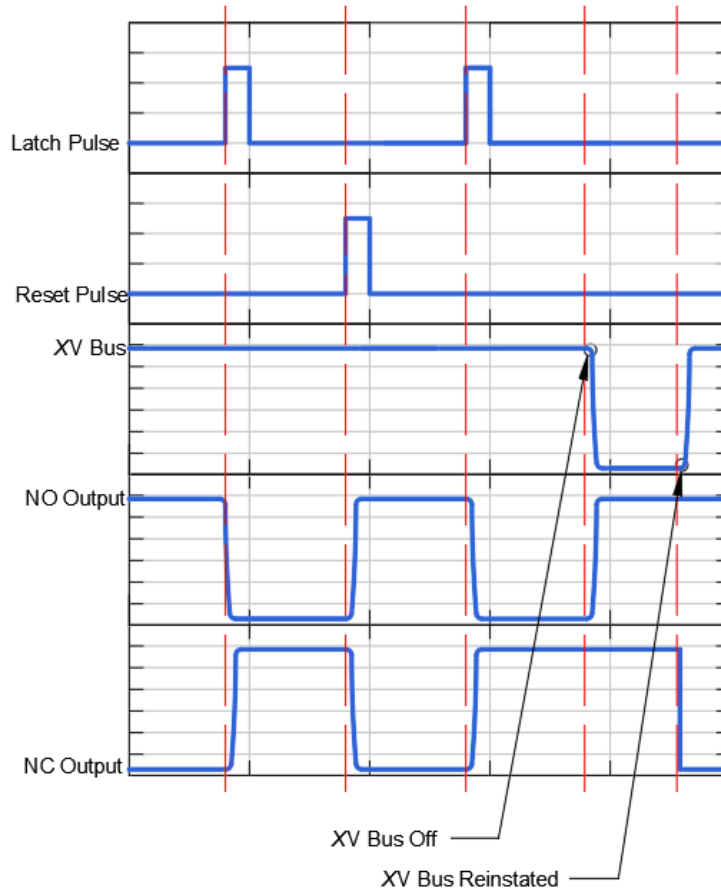
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APPLICATIONS

APPLICATION 1

Notes:

- For low side switching
- All loads connected to *X*V
- *X*V Bus Return has the sum of current from all loads and *X*V PSU
- Waveforms below measured at points A1/B1 (NO) and A3/B3 (NC) outputs with respect to *X*VBus Return

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Notes:

- For low side switching
- Can have an XV power supply for a virtual V_{CC}
- VA and VB can be independent supplies (and lower than XV)
- Can also be expanded to independent PSUs on the loads of A3, A1, B3 and B1
- All output supplies must share the same ground
- XV Bus Return has the sum of currents from VA, VB and XV
- Waveforms below measured at points A1/B1 (NO) and A3/B3 (NC) outputs with respect to XVBus Return

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SELECTION GUIDE

Bus Voltage (V)	I$_D$ (A)	R$_{(ON)}$ (TYP) (mΩ)
10-50	1 3 5 10 15 20	10

ORDERING PARTS

CSMRLVG X X P1

Part Reference	Circuit	Current (A)	Package Type
CSMRLVGXXP1	A (SPST) B (SPDT)	1 3 5 10 15 20	8 Pin Lead Package

PACKAGE STYLES AND CONFIGURATION OPTIONS

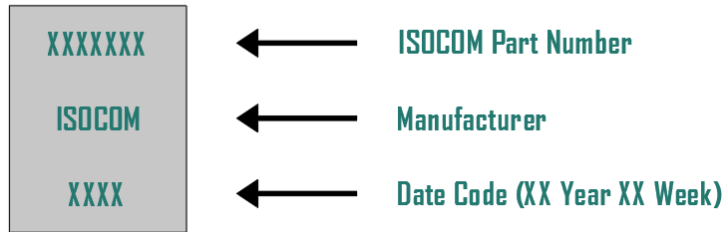| Package	8 Pin Lead
Lead Style	-
Channels	Optional
Common Channel Wiring	-
ISOCOM Part Number and Options	
Commercial	CSMRLVGXXP1
Defense Screen Level	CSMRLVGXXP1/L2
Space Screen Level	CSMRLVGXXP1/L2S
Standard Gold Plate Finish	Gold Plate
Solder Dipped	Option #20

DEVICE MARKING

FRONT OF DEVICE

XXXXXX ← ISOCOM Part Number

ISOCOM ← Manufacturer

XXXX ← Date Code (XX Year XX Week)

BACK OF DEVICE

XXX ← Serialisation

IXXXX ← Batch ID
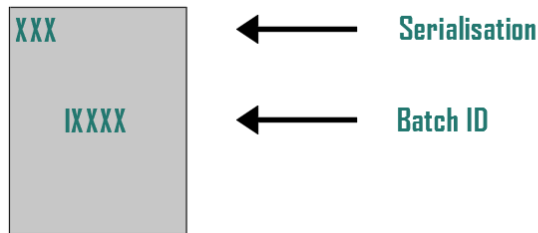
FOR SPACE SCREENED PARTS ONLY

OUTLINE DRAWINGS

8 Pin Lead Surface Mount
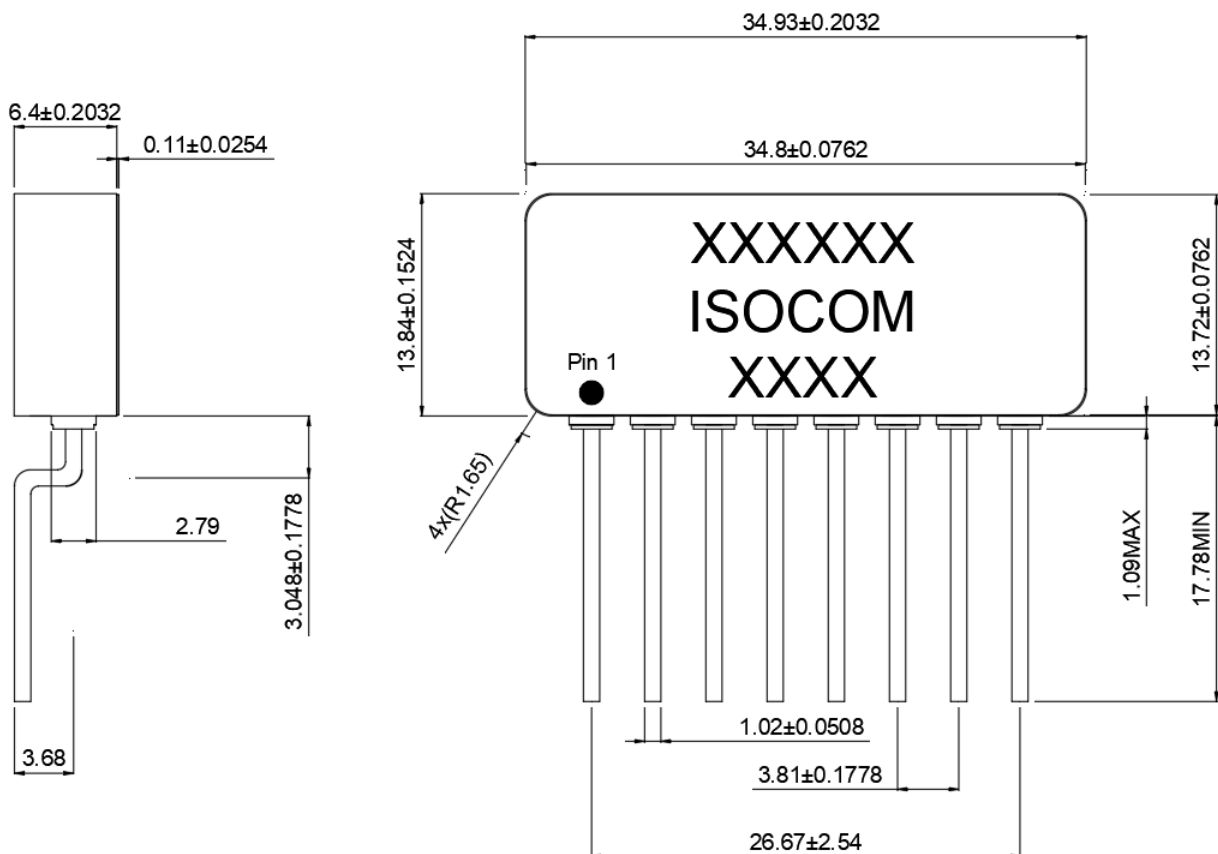
6.4±0.2032

0.11±0.0254

13.84±0.1524

2.79

3.048±0.1778

3.68

34.93±0.2032

34.8±0.0762

XXXXXX
ISOCOM
XXXX

Pin 1

13.72±0.0762

4x(R1.65)

1.09MAX

17.78MIN

1.02±0.0508

3.81±0.1778

26.67±2.54

PIN OUT INFORMATION

Pin Number	Pin Function	
	SPST	SPDT
1	NO1	NO1
2	Reset	Reset
3	GND	GND
4	Latch	Latch
5	XVBus	XVBus
6	XVBus Return	XVBus Return
7	XVBus Return	XVBus Return
8	N/C	NC1

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