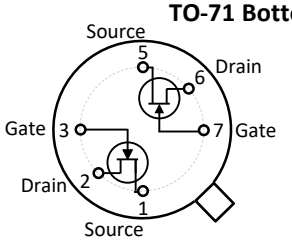
IF1322, IF1322A Dual Matched N-Channel JFET

Features

- InterFET N0132L Geometry
- Low Noise: 1.0 nV/√Hz Typical
- High Gain: 20mS Typical
- Low Cutoff Voltage: 1.5V Maximum
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

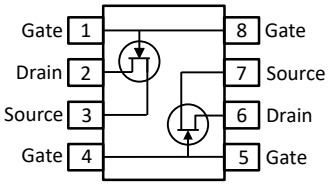
TO-71 Bottom View



Applications

- Low Noise High Gain Amplifier
- Differential Amplifiers
- Instrumentation Amplifiers
- Acoustic and Vibration Sensors

SOIC8 Top View



Description

The -20V InterFET IF1322 matched pair JFET is targeted for low noise high gain differential amplifier designs. The IF1322 has a cutoff voltage of less than 1.5V ideal for low-level power supplies. The TO-71 package is hermetically sealed and suitable for military uses. Custom specifications, matching, and packaging options are available.

Product Summary

Parameters		IF1322 Min	IF1322A Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-20	-20	V
I_{DSS}	Drain to Source Saturation Current	8	8	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.8	-0.8	V
G_{FS}	Forward Transconductance	10	10	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF1322T71; IF1322AT71	Through-Hole	TO-71	Bulk
IF1322S08; IF1322AS08	Surface Mount	SOIC8	Bulk
IF1322S08TR; IF1322AS08TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IF1322COT; IF1322ACOT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IF1322CFT; IF1322ACFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	400	mW
P	Power Derating	2.3	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C

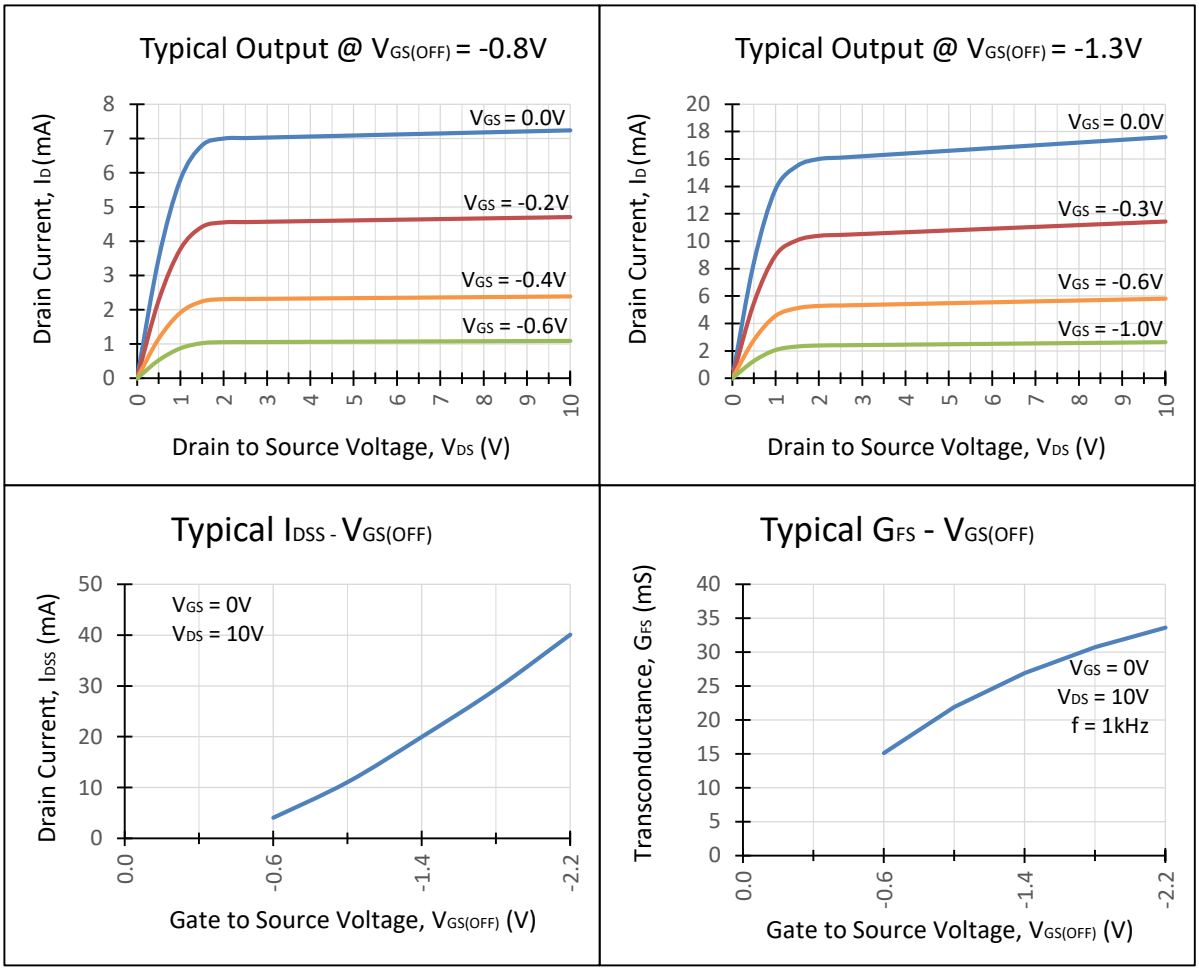
Static Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	IF1322		IF1322A		Unit
			Min	Max	Min	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	GSS1: I_G = -25µA, V_{DS} = 0V GSS2: I_G = -3µA, V_{DS} = 0V GSS3: I_G = -1µA, V_{DS} = 0V	-20		-20		V
I_{GSS}	Gate to Source Reverse Current	V_{DS} = 0V, V_{GS} = -10V		-0.1		-0.1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1µA	-0.8	-1.5	-0.8	-1.5	V
$V_{GS(F)}$	Gate to Source Forward Voltage	V_{DS} = 0V, I_G = -1mA V_{DS} = 0V, I_G = -1µA	0.3	1.0	0.3	1.0	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 10V, V_{GS} = 0V (Pulsed)	8	25	8	25	mA

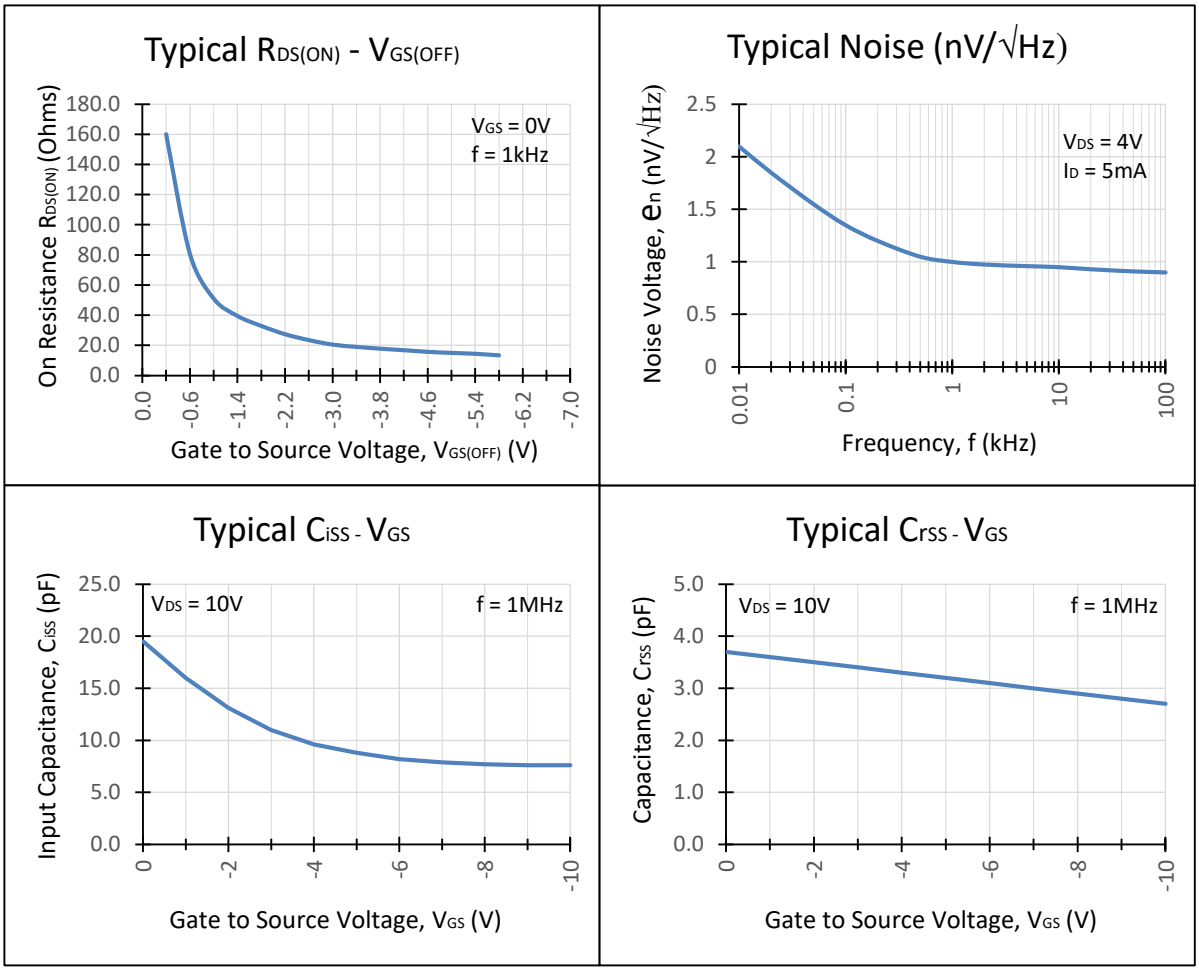
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	IF1322		IF1322A		Unit
			Min	Max	Min	Max	
G_{FS}	Forward Transconductance	V_{DS} = 5V, V_{GS} = 0V	10		10		mS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 5V, I_D = 3mA		30		40	mV
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 5V, I_D = 3mA, f = 1kHz V_{DS} = 5V, I_D = 3mA, f = 100Hz		2 4		2 4	nV/√Hz
i_n	Equivalent Circuit Input Noise Current	V_{DS} = 5V, I_D = 3mA, f = 1kHz		0.05		0.05	pA/√Hz

Typical IF1322, IF1322A Characteristics

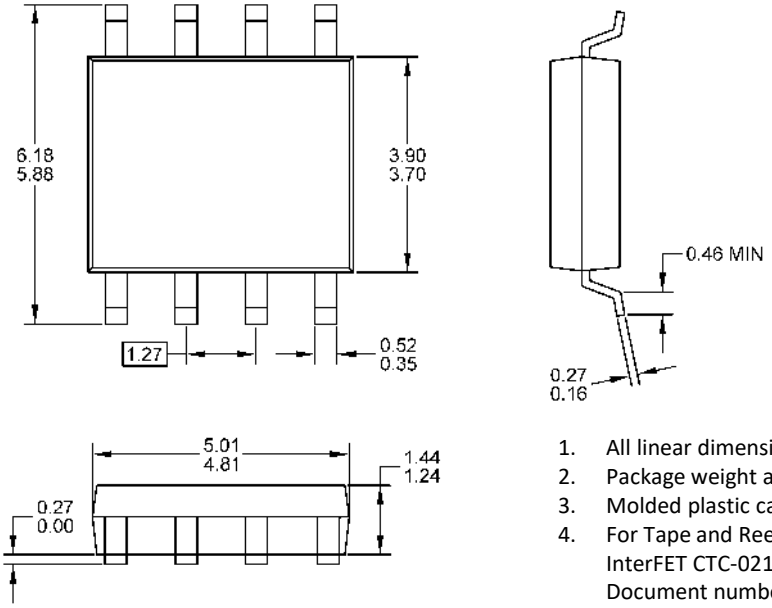


Typical IF1322, IF1322A Characteristics (Continued)



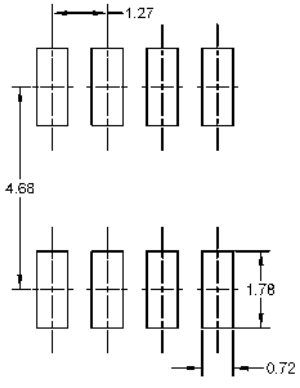
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

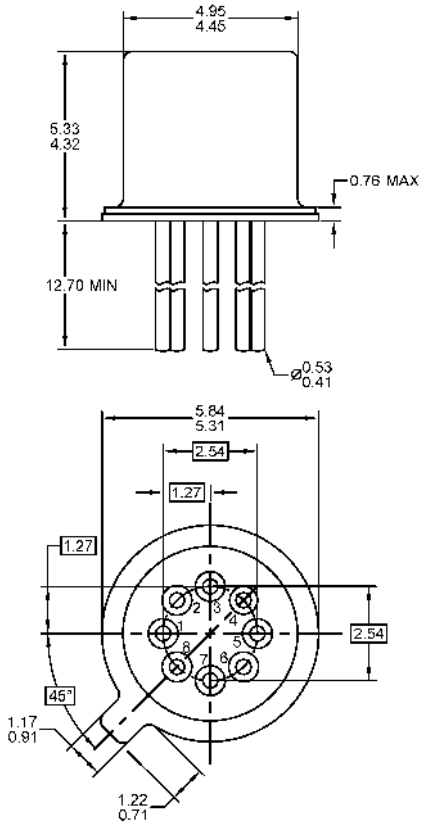
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

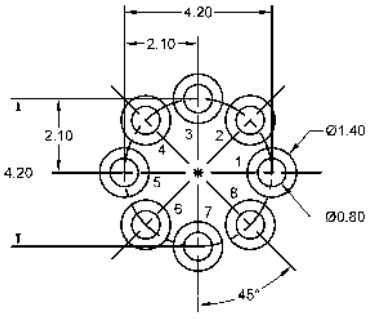
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.